Date: Wednesday, 04/Dec/2019

Time	Session				
8:00am - 9:00am	**Registration 01** Location: **Jasmine Foyer**				
9:00am - 10:30am	**PDC 1: Power Electronics Packaging for Automotive Applications** Location: **3811** Prof. Mervi Paulasto-Kröckel; Aalto University	**PDC 2: Fan-Out Wafer/Panel-Level Packaging and Heterogeneous Integrations** Location: **3812** Dr. John H Lau, Unimicron Technology Corporation	**PDC 3: Reliability Mechanics and Modeling for IC Packaging - Theory, Implementation and Practice** Location: **3813** Prof. Xuejun Fan, Lamar University	**PDC 4: Antenna-in-Package (AiP) Technology for Millimeter Wave Systems** Location: **3911** Prof. Y. P. Zhang, Nanyang Technological University	**PDC 5: Co-Design/Modeling and Additive Manufacturing for Electronics Packaging** Location: **3912** Prof. Christopher Bailey, University of Greenwich
10:30am - 11:00am	**Coffee/Tea Break-01** Location: **Lunch Hall (3610/3611/3612/3710/3711/3712)**				
11:00am - 12:30pm	**PDC 1-: Power Electronics Packaging for Automotive Applications** Location: **3811** Prof. Mervi Paulasto-Kröckel; Aalto University	**PDC 2-: Fan-Out Wafer/Panel-Level Packaging and Heterogeneous Integrations** Location: **3812** Dr. John H Lau, Unimicron Technology Corporation	**PDC 3-: Reliability Mechanics and Modeling for IC Packaging - Theory, Implementation and Practice** Location: **3813** Prof. Xuejun Fan, Lamar University	**PDC 4-: Antenna-in-Package (AiP) Technology for Millimeter Wave Systems** Location: **3911** Prof. Y. P. Zhang, Nanyang Technological University	**PDC 5-: Co-Design/Modeling and Additive Manufacturing for Electronics Packaging** Location: **3912** Prof. Christopher Bailey, University of Greenwich
12:30pm - 2:00pm	**Lunch 01: Lunch** Location: **Lunch Hall (3610/3611/3612/3710/3711/3712)**				
2:00pm - 2:20pm	**Opening Ceremony** Location: **Main Hall (3803/3804/3805/3903/3904/3905)**				
2:20pm - 3:00pm	**Keynote 01: Innovation in Electronic Packaging for Compute and Communication** Location: **Main Hall (3803/3804/3805/3903/3904/3905)** Dr. Ram Viswanath, Intel				
3:00pm - 3:40pm	**Keynote 02: Enabling the Building Blocks for Next Generation of Electronic Packaging** Location: **Main Hall (3803/3804/3805/3903/3904/3905)** Mr. Glen Mori, Applied Materials				
3:40pm - 4:15pm	**Coffee/Tea Break-02: Exhibitor Presentation I** Location: **Exhibition Hall (3801/3802/3901/3902)**				
4:15pm - 6:15pm	**Panel Session: Packaging Material Challenges & Opportunities for 5G Applications** Location: **Main Hall (3803/3804/3805/3903/3904/3905)**				

Date: Thursday, 05/Dec/2019

Time					
8:00am - 9:00am	**Registration 02** Location: **Jasmine Foyer**				
9:00am - 9:30am	**Invited-01: Manufacturing Technology Solution of Small Via for Heterogeneous Integration** Location: **3811** Dr. Yasuhiro Morikawa, ULVAC	**Invited-02: Market and Technology Trends of Advanced Packaging, Fan-Out Packaging** Location: **3812** Favier Shoo, Yole Development	**Invited-03: Highly Accurate, Efficient and Reliable Silicon Photonics Wafer Level Test and Characterization** Location: **3813** Dr. Sia Choon Beng, FormFactor Inc.	**Invited-04: Reduction of Aging Induced Reliability Degradations Using SAC+X Lead Free Solders** Location: **3911** Prof. Jeffrey Suhling, Auburn University	**Invited-05: Cooling of High Power Microelectronic Components using Flow Boiling** Location: **3912** Prof. Yogendra Joshi, Georgia Institute of Technology
9:30am - 10:30am	**A1: 2.5D, 3D and TSV Processes - I** Location: **3811**	**A2: Wafer Fan-Out Processes - I** Location: **3812**	**A3: LED and Photonic Packaging** Location: **3813**	**A4: Advancement in Solder Joint Characterization and Reliability - I** Location: **3911**	**A5: Thermal Characterization and Cooling Solutions - I** Location: **3912**
10:30am - 11:15am	**Coffee/Tea Break-03** Location: **Exhibition Hall (3801/3802/3901/3902)**		**Interactive: Interactive Session** Location: **Jasmine Foyer**		
11:15am - 12:35pm	**B1: 2.5D, 3D and TSV Processes - II** Location: **3811**	**B2: Wafer Fan-Out Processes - II** Location: **3812**	**B3: Sensors & IoT Packages** Location: **3813**	**B4: Advancement in Solder Joint Characterization and Reliability - II** Location: **3911**	**B5: Thermal Characterization and Cooling Solutions - II** Location: **3912**
12:35pm - 2:05pm	**Lunch 02: EPS Luncheon** Location: **Main Hall (3803/3804/3805/3903/3904/3905)**				
2:05pm - 2:35pm	**Invited-06: Innovative Package Solution for 5G Era** Location: **3811** Dr. Yu-Po Wang, SPIL	**Invited-07: Evolution of Fault Isolation Techniques for Product Failure Analysis** Location: **3812** Dr. Goh Szu Huat, GlobalFoundries	**Invited-08: Micro Interconnects: Signal Integrity in 5G Applications** Location: **3813** Dr. Murali Sarangapani, Heraeus Materials	**Invited-09: Development of Novel Polymer Materials for Advanced Packaging** Location: **3911** Dr. Takenori Fujiwara, Toray Industries	**Invited-10: Virtual Prototyping for Electronic Packaging Development, Dream or Reality?** Location: **3912** Dr. Jing-En Luan, ST Electronics
2:35pm - 3:35pm	**C1: 2.5D, 3D and TSV Processes - III** Location: **3811**	**C2: Advanced FA and Reliability Characterization** Location: **3812**	**C3: Next Generation Wirebonding & Characterization** Location: **3813**	**C4: Assembly Materials and Processing - I** Location: **3911**	**C5: Thermal Characterization and Cooling Solutions - III** Location: **3912**
3:35pm - 4:20pm	**Coffee/Tea Break-04: Exhibitor Presentation II** Location: **Exhibition Hall (3801/3802/3901/3902)**				
4:20pm - 5:40pm	**D1: Silicon and Glass Interposer** Location: **3811**	**D2: Advanced Substrate Materials** Location: **3812**	**D3: Silver Sintering for Power Modules** Location: **3813**	**D4: Assembly Materials and Processing - II** Location: **3911**	**D5: Thermal Characterization and Cooling**

					Solutions - IV Location: 3912
5:40pm - 6:00pm	**Reception** Location: Exhibition Hall (3801/3802/3901/3902)				
6:00pm - 7:45pm	**Workshop: Heterogeneous Integration Roadmap** Location: Main Hall (3803/3804/3805/3903/3904/3905)				
8:00pm - 10:30pm	**Conference Banquet** Location: Club 55				
Date: Friday, 06/Dec/2019					
8:30am - 9:00am	**Registration 03** Location: Jasmine Foyer				
9:00am - 9:30am	**Invited-11: A Comprehensive Reliability Assessment on 2.5D and 3D Integration** Location: 3811 Premachandran C.S., GlobalFoundries	**Invited-12: System Packaging Solutions for High-Performance Computing in the Era of 5G/IoT** Location: 3812 Shunichi Kikuchi, Fujitsu Advanced Technologies	**Invited-13: Plasma Process Optimization for Cu Bonding Integration using the Design of Experiment Technique** Location: 3813 Prof. Sarah Kim - Seoul National University of Science and Technology	**Invited-14: Novel MEMS-based Lateral Contact Probing Method for Fine Pitch Micro-bumps for High Bandwidth Memory (HBM) Testing** Location: 3911 Dr. Daniel Rhee Min Woo, Samsung	**Invited-15: Importance of Warpage Engineering in the Era of Heterogeneous Integration** Location: 3912 Prof. S.B. Park, State University of New York at Binghamton
9:30am - 10:30am	**E1: New Interconnects for 3D and Heterogeneous Integration - I** Location: 3811	**E2: RF, 5G & mmWave Packaging - I** Location: 3812	**E3: Hybrid Bonding** Location: 3813	**E4: Packages Quality, Reliability & Modeling** Location: 3911	**E5: Thermal-Mechanical Simulation for Advanced Packages - I** Location: 3912
10:30am - 11:15am	**Coffee/Tea Break-05: Exhibitor Presentation III** Location: Exhibition Hall (3801/3802/3901/3902)				
11:15am - 12:15pm	**F1: New Interconnects for 3D and Heterogeneous Integration - II** Location: 3811	**F2: RF, 5G & mmWave Packaging - II** Location: 3812	**F3: Electrical Simulation for Advanced and Emerging Packages - I** Location: 3813	**F4: Thermal Characterization and Cooling Solutions - V** Location: 3911	**F5: Thermal-Mechanical Simulation for Advanced Packages - II** Location: 3912
12:15pm - 1:45pm	**Lunch 03: EPTC Luncheon** Location: Main Hall (3803/3804/3805/3903/3904/3905)				
1:45pm - 2:15pm	**Invited-16: Material Advancement for Heterogeneous**	**Invited-17: Development of Multi-chip Integration Non-Molded 2.5DIC**	**Invited-18: Memory-Centric Design Challenges for**	**Invited-19: Effects of Trace Element on Electromigration of FC**	**Invited-20: Will Lidded or Lidless Advanced Packaging Have Better Thermo-**

	Integration Location: **3811** Dr. Dongshun Bai, Brewer Science	**Packaging** Location: **3812** Dr. Chen Wei Chung, ASE Global	**Flash Products** Location: **3813** Dr. Gokul Kumar, Micron	**Interconnect between Cu Pillar and Sn-Bi Alloy** Location: **3911** Murayama Kei, Shinko Electric Japan	**Mechanical Characteristics?** Location: **3912** Dr. Gamal Refai-Ahmed, Xilinx
2:15pm - 3:15pm	**G1: New Interconnects for 3D and Heterogeneous Integration - III** Location: **3811**	**G2: RF, 5G & mmWave Packaging - III** Location: **3812**	**G3: Electrical Simulation for Advanced and Emerging Packages - II** Location: **3813**	**G4: Power Module Assembly and Technologies - I** Location: **3911**	**G5: Thermal-Mechanical Simulation for Advanced Packages - III** Location: **3912**
3:15pm - 4:00pm	**Coffee/Tea Break-06: Exhibitor Presentation IV** Location: **Exhibition Hall (3801/3802/3901/3902)**				
4:00pm - 5:40pm	**H1: New Interconnects for 3D and Heterogeneous Integration - IV** Location: **3811**	**H2: RF, 5G & mmWave Packaging - IV** Location: **3812**	**H3: Electrical Simulation for Advanced and Emerging Packages - III** Location: **3813**	**H4: Power Module Assembly and Technologies - II** Location: **3911**	**H5: Printed Electronics & 3D Printing** Location: **3912**
5:40pm - 6:00pm	**Closing Ceremony: Conclusion & Lucky Draw** Location: **Main Hall (3803/3804/3805/3903/3904/3905)**				